Yield and Reliability Challenges at 7nm and Below

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Abstract

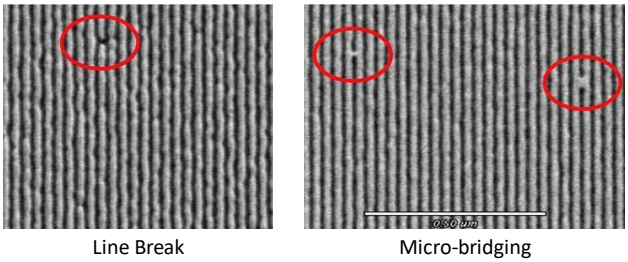
Layout Design Rules have been scaled very aggressively to enable the 7nm technology node without EUV. As a result, achieving acceptable performance and yield in High Volume Manufacturing (HVM) has become an extremely challenging task. Systematic yield and parametric variabilities have become quite significant. Moreover, due to overlay tolerance requirements and diminishing process windows, reliability risks due to soft shorts/leakages and soft opens for both FEOL and BEOL have also increased to a critical level. Introduction of EUV at the second wave of 7nm and 5nm will not help significantly due to increased defectivity and significant increases in Local Edge Roughness. New characterization techniques are necessary to identify the yield and reliability risks. After reviewing the evolution of design rules and classifying the yield and reliability risks, we will present examples from Design-For-Inspection™ (DFI™) and the novel VarScan methodology to "detect the undetectable" defects and characterize variability for both FEOL and BEOL 7nm and below technologies.

Layout Design Rule Scaling Scenarios

Scaling FinFET-based technologies to 7nm and below nodes in the absence of EUV has been extremely difficult and requires multiple patterning. Although Self Aligned Multiple Patterning (SAMP) enables printing of 1-directional grating patterns, the cut masks for both FEOL and BEOL pose a huge challenge in terms of Edge Placement Error (EPE). This results in increased variability and reduces the process windows to a dangerous level. For layout patterns with multiple mask levels, EPE can be described by the following equation:

$$\sigma_{EPE} \approx \sqrt{\sum_{i=1}^{n}\left(\frac{\sigma_{CD(i)}}{2}\right)^2 + \sum_{j=1}^{n-1}\sigma_{Overlay(j)}^2} + \beta$$

where n is the number mask levels in the layers under consideration and β is the systematic variability in printing the lines and cuts [1]. Typical 3σ CD variability for the Fin Cuts can be 30% of the pitch and 20% of the pitch for the BEOL Mx Block. Corresponding μ +/-3σ overlay ranges can be 60% and 40%, respectively. So if we assume 3nm CDU for the cuts and 6nm for the mix-match overlay, for 2 Block Masks we will get σ_{EPE} of 9nm and for 4 Block Masks 13nm [1]. Although the lithographic sources of variations dominate, especially overlay, but also CDU, dose/focus and Mask Enhancement Error Factor (MEEF), the contribution of non-lithographic sources such as aspect ratio and pattern density etch, CMP and film stress play an important role as well. This variability picture is even more scary if we consider wafer spatial distributions especially at the wafer edge.



Line Break Micro-bridging

Fig 1. EUV introduces new defectivity challenges

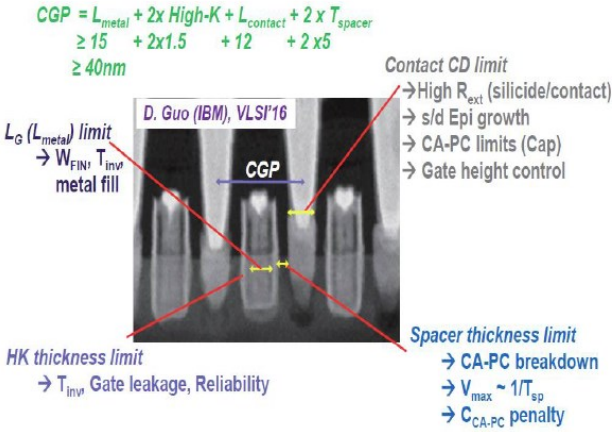


Fig. 2 Contacted Gate Pitch Scaling Challenges

With the introduction of EUV scanners in the second wave of 7nm or 5nm, assuming the same overlay tolerances as the most advanced 193 immersion scanners, the cut or Block variability will be significantly reduced. However, the local CD variations due to small number of photons will be significantly increased (the so-called shot noise or stochastic effects) and the EPE will be still a significant issue. New sources of EUV-related mask and wafer defectivity introduce additional challenges [9] (See Fig. 1).

Without any doubt, the most challenging design rule is the spacing between Gate and Source/Drain. Since the L_{gate} and the contact to the active area could not be scaled very aggressively, and the Contacted Gate Pitch (CGP) had to be scaled, the spacing had to be reduced to almost the absolute limits as it is shown in Fig. 2 [2].

As shown in this figure, the CGP will have to remain around 40nm and L_{gate} will not scale beyond 12nm due to fill width and thickness for the Work Function (WF) and acceptable Gate Resistance. To get adequate electrostatic control, fin width has to be reduced but cannot be much smaller than 5nm. Also, to keep an acceptable value of the contact resistance, contact width has to be kept above 10mn. So, it's clear that we are reaching the limits of FinFET capabilities and the new Gate All Around (GAA) architectures will have to be introduced.

Another effective scaling scenario for standard cells was the introduction of the Single Diffusion Break instead of the Double Diffusion Break by Samsung in their 14nm technology node. This was also implemented by Intel in their 10 nm process which is virtually equivalent to the foundry 7nm technology [3] (See Fig. 3). However, this technique is still vulnerable to the overlay variations in the cut mask.

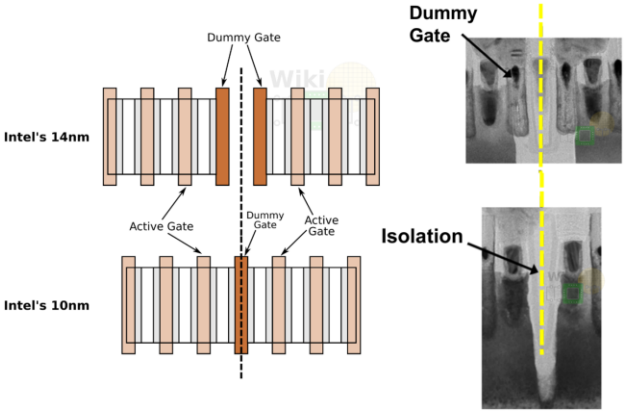


Fig. 3 Transition to Single Diffusion Break

Challenges in Identifying Yield and Reliability Detractors

These aggressive scaling scenarios have severe consequences in terms of yield detractors. In particular, while the fabs have been able to clean up the equipment and process related random defectivity, systematic and parametric detractors dominate the yield losses. Conventional inline monitoring techniques cannot catch the subtle electrical signatures of these yield and reliability issues and new methods are needed. We will show now several examples of the potential yield loss detractors caused by challenging EPE/overlay requirements. Figure 4 illustrates this for the case of gate to S/D spacing violations [4]. If there is an electrical leakage path as shown in the red circle, it cannot be detected by the optical or top SEM inspection.

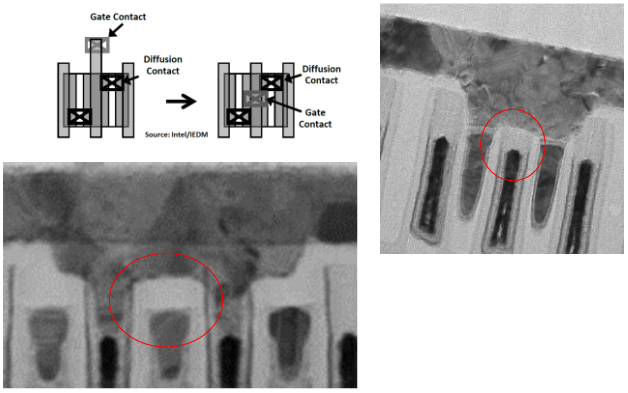


Fig. 4 Gate to S/D spacing: leakage path

The same difficulty exists in the Metal Gate Poly Cut Mask as shown in Fig. 5 [5], however the failure mode is different from the one above. The result is a shift in the transistor threshold voltage which may result in a parametric failure.

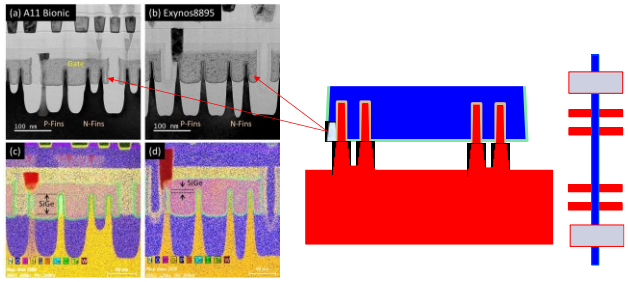


Fig. 5 Metal Gate Poly Cut Mask Defect

Our final example presents via to under metal leakage due to chamfering [8] (See Fig. 6). Similar integration schemes are also used for the first metal vial layer (V0) and can result in gate-to-drain leakages or shorts.

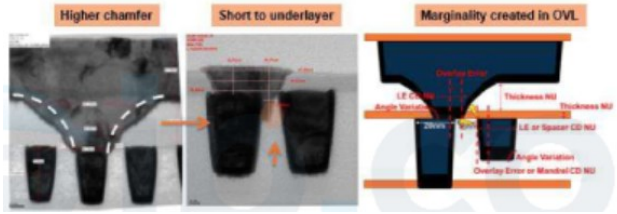


Fig. 6 Via Chamfering and shorts to under-layer

While these effects may be causing yield losses at time t=0, i.e., at wafer sort, the soft shorts or leakages due to extremely small spacing as a result of process variations can be the root cause of reliability failures. These soft shorts and leakages must be identified as early as possible to prevent excessive failures during burn-in or, even worse, in the field when the chips are put in the system. This has become critical for systems with zero-defect requirements such as automotive or other long lifetime applications.

Figure 7 illustrates this effect for via to metal chamfering leakage due to overlay or misalignment variations [6].

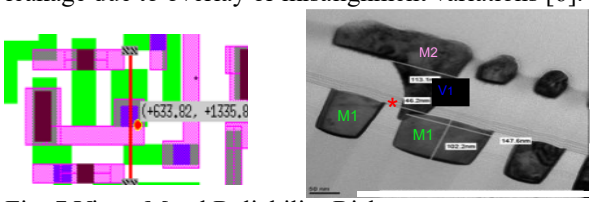


Fig. 7 Via to Metal Reliability Risk

With 100 million worst-case vias on a 20nm chip, if 10nm is the minimum spacing required to guarantee product lifetime reliability, chip failure would be about 240 DPPM if the standard deviations (σ's) of nth via (VIAn) and nth metal (Mn) layer critical dimensions (CDs) are controlled at 2.0nm and 1.4nm, respectively, and the VIAn-to-Mn alignment σ is as tight as 2.3nm [6].

Similarly, soft open via or contact failures may be reliability risks as well. Their identification on the ppm level is quite challenging and requires a new methodology. In 7nm technology node, contact resistance variability is a big issue and must be detected by extracting the resistance distributions and identifying the outliers for entire wafers including wafer edges where these issues are most pronounced.

Design-For-Inspection Solution

We have developed a new methodology called Design-for-Inspection (DFI) that enables sensitive inline pickup for failure mechanisms previously undetectable until product test (wafer sort, final test, HTOL) or field failures. DFI is taking advantage of otherwise unused space within the product die, and as well as within the scribe lines between the die [7]. Figure 8 illustrates the components of the system, including high density DFI Filler cell test structures, the custom-built eProbe® E-beam tool for high speed, non-contact inline measurement, and the Exensio analytics solution, linking the billions of DFI filler cell responses from each wafer with other fab and product data for efficient diagnostics, trending and control.

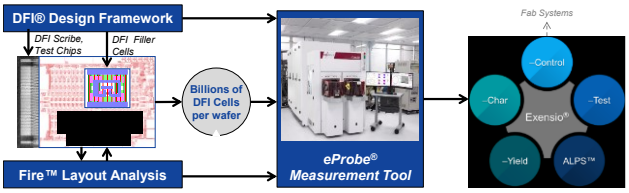


Fig. 8 Design-For-Inspection system

The DFI system is particularly useful for detecting the small leakages that plague 7nm process integration schemes. A key example, described above, is gate-to-S/D leakage, which dominates initial yield losses in the technology ramp and remains a reliability risk even in mass production. Such leakages are sometimes detectable only with high voltage stress during product test and even then may be missed and cause field failures. DFI enables sensitive pickup for these leakages as early as the first contact and metallization layers. Figure 9 illustrates how high speed eProbe measurement detected subtle shifts in the Electrical Response Index (ERI) which were later validated by electrical failure analysis. Such inline capability creates new opportunities for foundries and their fabless customers to collaborate for product success.

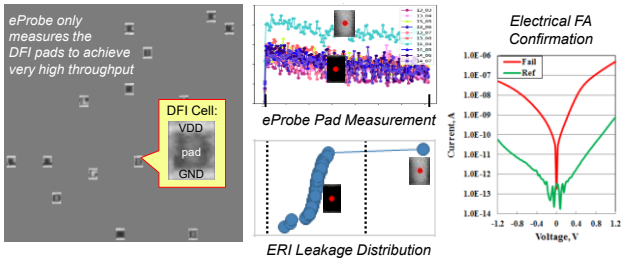


Fig. 9 eProbe Leakage Measurements Validation

VarScan Solution

To identify contact and via ppm level variability from 1 kΩ to 10 MΩ range, we have developed a new system called VarScan shown in Fig. 10. It consists of an ultra-high density resistor/transistor array that can be placed either in MPW or in the volume production Scribe.

In the 60µm Scribe-line, the total chip length is 2mm and in the 7nm technology each macro contains either 50k resistors or 150k transistors.

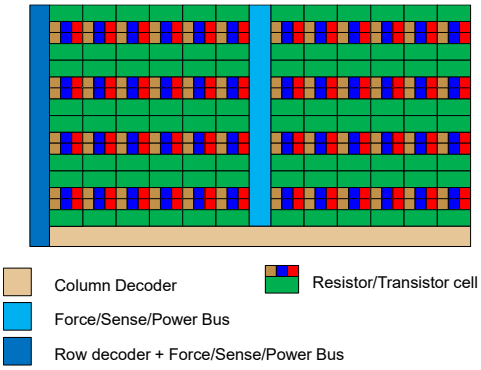


Fig. 10 VarScan Resistor/Transistor Array Layout

These structures are tested on PDF's highly parallel pdFasTest® system and all scribe-line structures for all wafers in a lot for a given failure more can be measured in less than 2 hours (within the allowed queue time) providing an unprecedented observability of 1ppm to 100ppb parametric defect detection capability. First implemented for passive resistors, this capability was then applied to transistor variability in VarScan-II (See Fig. 11).

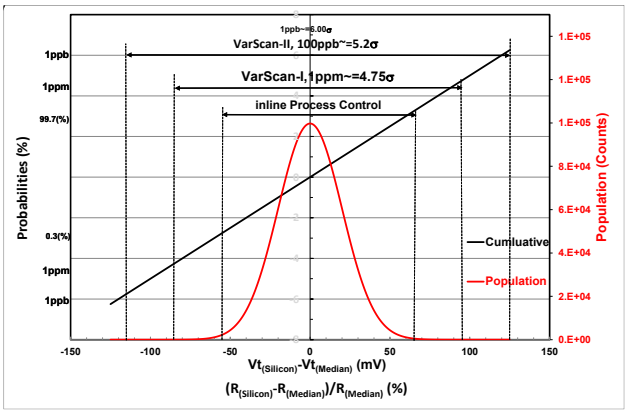


Fig. 11 VarScan I & II Parametric Defect Detection Capability

Conclusions

In this paper we described how the aggressive scaling of layout design rules in 7nm technology node led to the vulnerability of systematic and parametric yield loss detractors and moreover to the significant increase in reliability risks. New methodologies are needed since these detractors cannot be identified by the standard optical, SEM or E-beam systems. We have introduced two new approaches, Design-For-Inspection and VarScan, which have been successfully implemented in leading foundries and fabless companies, to provide the detection capabilities required to achieve successful volume manufacturing yield and reliability levels in the 7nm and below technologies.

Acknowledgements

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