Characterization Challenges and Solutions for FDSOI Technologies

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***Abstract* — FDSOI technology has been proposed as an alternative device scaling path which offers benefits of tunable, superior electrostatics transistor while maintaining simplicity of planar integration. New device type and integration elements brought up challenges in device and process characterization and monitoring across the whole lifecycle of the technology. This paper presents successful application of fast cycle-time electrical characterization to ramp FDSOI technology to mass production.**

Keywords— FDSOI, Technology Development, Yield Ramp, Characterization Vehicles, Electrical Characterization, Test Chip

I. INTRODUCTION

At the dawn of 20nm node, short channel effects and channel leakage threatened further transistor scaling. Most attractive solution was proposed in the form of fully depleted devices, with either planar Ultra-Thin-Body or 3-dimentional tri-gate FinFET architecture [1]. FinFET was first introduced by technology leaders for High Performance Logic IC's [2] and adopted by major foundries at 16/14nm. Fully-Depleted Silicon-on-Insulator (FDSOI) technology was originally adopted at 28nm [3], with next nodes developed down to 14nm [4]. Both technologies introduced new integration elements (FDSOI to less extent) which posed challenges for technology development, yield ramp, and mass production. Characterization tools, including electrical test, metrology, and inspection were adopted to help addressing those challenges. For electrical device and module characterization, we adopted a comprehensive solution, which utilized complete set of test structures with ultra-fast test and data acquisition to support FDSOI technology through all phases of its lifetime.

In the paper, we first introduce the FDSOI technology, its capabilities, advantages, and integration challenges. Then we describe the components of the characterization toolset to collect process relevant data using electrical tests from Characterization Vehicles (CVs). Finally we will show the usage of characterization tools across phases of technology life.

II. FDSOI TECHNOLOGY

The concept of multi-gate fully depleted channel transistor has been proposed more than 30 years ago, and decades of university and industrial research resulted in very elegant solution in the form of current FDSOI transistor.

Thin silicon body with the Ground Plane acting as a second gate eliminates the need for channel doping, thus reducing Vt and operating voltage, increasing mobility, and reducing variability due to use of undoped channel. Better electrostatics suppresses Short-Channel Effects and enables gate length scaling. Planar integration is compatible with multiple performance boosters – channel strain, dual channel for NMOS/PMOS mobility, and multiple work-function metals integrated with gate-first approach for Hi-K/MG stack. Isolated well regions, which serve as ground planes, also provide a unique capability to apply back-bias for Vt tuning.

With current integration and additional boosters, 28nm and 22nm FDSOI technologies are in mass production, with next node development already announced and scaling path identified down to 10nm node.

FDSOI uses planar integration which offers a significant benefit - it allows keeping all the traditional elements developed and mastered during multiple generations of planar SOI technologies. Key differences between FDSOI and other planar technologies include thin-Si/thin-Buried Oxide substrate, faceted raised Source/Drain epitaxial regions, and Hybrid Bulk/FDSOI device co-integration. The new elements introduce new systematics, failure modes, and defects, and require extensive characterization to drive improvement to achieve desired performance and high product yields [5-8].

Many challenges had been identified and addressed before qualification and mass production, and the original technology grew to offer a platform for new solutions.

III. CHARACTERIZATION VEHICLE INFRASTRUCTURE

One of the development tools used to accelerate FDSOI bring-up was CV infrastructure, historically well suited to support development and ramp of new technologies. In case of 28nm FDSOI, some technology elements and modules were based on 28nm "Bulk" process, adopting many design rules and taking advantage of many process modules (including already existing BEOL metallization scheme). CV-based solution can help technology development and process optimization by targeted characterization of systematics and defectivity. Typically, SRAM and other IP blocks provide feedback on fully integrated functionality and performance, while CVs allow decomposing the integrated flow and focusing on the issues and failure modes at the layer and module level.

Characterization Vehicles incorporate a complete set of structures to characterize modules, defects, and devices. It incorporates many types of test structures (DUTs – Device Under Test) – some designed to capture systematic open or short failures across design space, other to characterize random defectivity. Depending on maturity of the technology and desired observability the DUTs can be implemented in direct multi-terminal passive test configuration or as an addressable array of DUTs [9-11], which increases the DUT density and test speed. Fast, multi-channel parametric tester, specifically

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designed for CV testing, enables 20-100 time test speed-up compared to traditional solutions. High parallelization of the test is also a key factor enabling parametric test of millions of transistors tested using Direct Probe CV implemented on top of partially processed product wafers [12].

CV's generate very large amount of data. The analysis is streamlined based on the pre-configured flow, using PDF Solutions Exensio Big Data platform [13], as shown in Fig. 1.

Table.1 Characterization Vehicle types and usage

CV Type	Placement	Application	Focus
FEOL/MOL CV	Stand alone or MPW	Development	Design Rule check Device Perf./Leakage Failure modes and Process Window
BEOL CV	Stand Alone	Validation and Yield Ramp	Defectivity reduction
Direct Probe CV (DPCV)	on Product	New Product Intro and Yield Ramp	Silicon-model matching Device LLE, Variability
Scribe CV	on Product	Mass Production	Process Monitor

Table 1 presents the suit of CV's used during technology bring-up and production phase. Some of the CV structures are only used in CV's dedicated to development phase, or during new product bring-up, while others can serve across the whole cycle, to support process monitoring during mass production.

Typical CV usage during development phase and early ramp is shown in Fig. 2. The benefit of CVs for this application is their unique capability to detect failures, separate them by module and layer, and pinpoint possible mechanisms. This is achieved using test structures with rich layout DoE (design of experiment), covering wide design space and many design attributes. Fast, multi-channel parametric tester tests all structures and collects parametric and functional responses across all terminals. The resulting data gives information about failure mechanisms, fail rates and parametric performance of all modules and devices.

IV. FDSOI Characterization

As a result of strong interaction and close cooperation between module integration, unit process, device engineering, and characterization teams we have demonstrated a strong and robust technology. CV wafers were used as a short loop with fast learning rate to, among others, check design rules, validate integration, and identify killer defects. Multiple failure modes were characterized using CV infrastructure, margins explored, and process windows implemented to ensure good performance and high yield in mass production under typical process variability. In addition to standard in-line process control procedures, enhanced electrical scribe line CV (process control monitors) have been implemented on multiple products to understand product sensitivities and further enhance process monitoring.

Scribe CV data from large set of wafers helped to identify specific product-dependent yield sensitivities. It also enabled to correlate them to in-line metrology parameters and set yield-relevant specs. Finally, CV data can be coupled with process parameters and production tool sensor signals, thus improving tool control and helping to optimize maintenance cycle.

Among many integration features and modules in FDSOI technology, some required dedicated test structures and characterization approach.

One of the examples is the SOI substrate with ultra-thin silicon layer on top of thin buried oxide layer, which is a key enabler and building block of FDSOI devices. Thickness and quality of both layers are of extreme importance for transistors and need to be monitored at all stages of manufacturing. Wafer suppliers have made great progress in substrate process control and initial wafer quality [14-15]. However, the impact of subsequent fabrication steps, process-induced silicon loss, as well as final uniformity and variability still need to be measured and monitored. Traditional metrology cannot easily be applied - only electrical methods can provide information about physical properties on micro and macro scale with the required speed and resolution.

We designed a dedicated electrical monitor applicable to development and mass production. It uses the approach similar to that proposed in [16], by using large array of small transistors and calibrating variability of their parameters with capacitances measured on neighboring structures. Test results from millions of transistors and capacitors produce electrical map of local and global thickness variation for silicon and buried oxide. This methodology was used during development and ramp to characterize process-induced silicon loss and minimize variability across wafer and die area. It can also be used by placing structures in Scribe area of product wafers as process monitor. Fig. 3 shows example of Si-thickness variation and corresponding Vt pattern across fully processed wafer, collected during process development stage.

Transistor variability can be driven by multiple factors, understanding them requires characterization of devices across wide range of layout configurations and across process corners. To investigate such effects we adopted Direct Probe CV [12], which uses a product (or IP block) design layout containing wide variety of device design styles. The transistors selected across the product die become a part of large set of DUTs, which are then tested across the die and across the wafer. Example of DPCV application is shown in Fig. 4, where the device performance is compared to their model values. The data was used to improve the model accuracy and validate process changes.

DPCV can also be used to detect variability of Source/Drain resistance. There are multiple types of test structures which can be used to characterize epi-grown S/D regions. For variability assessment, electrical test allows detection of minor shifts in Source/Drain resistance, but requires testing of large number of transistors. To separate various failure modes observed in early development stage we used a combination of contact chains and active/diffusion continuity structures. Fig. 5 shows failure rate correlation between these two types of test structures - the common failure mode may be caused by the defects related to epi S/D region.

To summarize, we demonstrated successful development of new family of silicon technology - FDSOI – with combination of multiple characterization tools, including CV infrastructure. New test structures and test techniques were developed and adopted to ensure full coverage of devices, modules, and failure modes.

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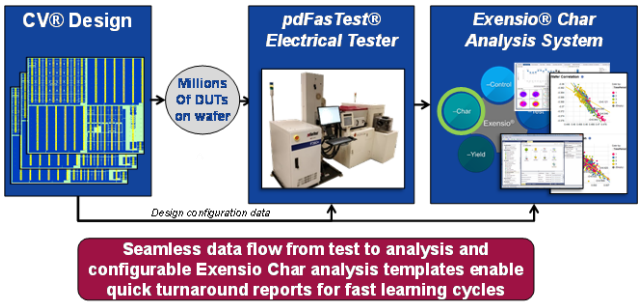

Fig. 1. Characterization Infrastructure with Characterization Vehicles, parallel tester, and Exensio analysis platform [13]

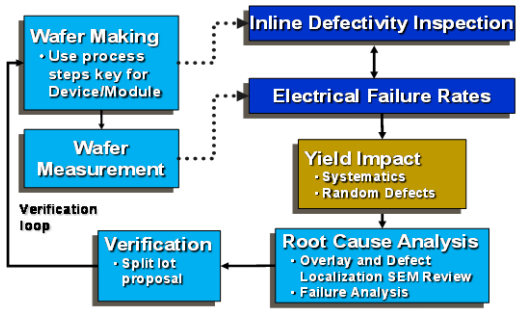

Fig. 2. Short Flow characterization loop using electrically testable structures on CV wafers.

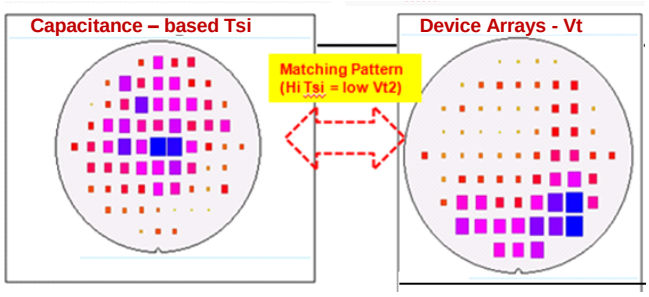

Fig. 3. Wafer level uniformity of Silicon Thickness extracted from Capacitance measurements and Vt variability in Transistor Arrays

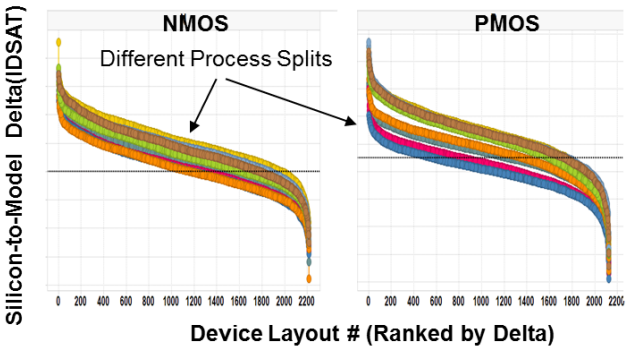

Fig. 4. Distribution of measured device performance (IDSAT) with respect to their model values for more than 2200 device layouts, NMOS and PMOS transistors. Direct Probe CV was used to collect the data from several wafers processed with different gate process conditions

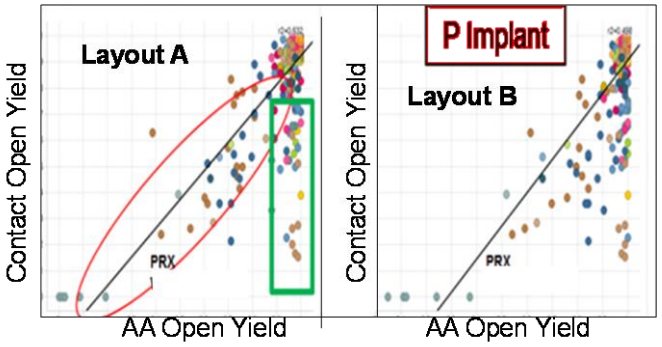

Fig. 5. Source/Drain region failure detection with a combination of Contact and Active monitor structures – correlation plots allow separation of failure modes at early development phase.