Novel E-beam Techniques for Inspection and Monitoring

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Abstract

In this paper, we report an advanced e-beam defect inspection tool (eProbe®250) and the Design-for-Inspection™ (DFI) system that has been built and deployed by PDF Solutions down to 4nm FinFET technology nodes. This tool has a very high throughput which allows for in-line inspection of nanometer level defects in the most advanced technology nodes. We also present eProbe applications for detection of systematic buried defects and process window characterization.
(**Keywords**: e-beam Inspection, FinFET, Yield)

Introduction

Actual yields achieved in advanced nodes quite often fall short with respect to their entitlement – mostly due to layout systematics and production variability. The nature of layout systematics has changed at advanced nodes. Many of the most impactful layout systematics are not detectable, since the resultant defects reside below the surface of the wafer. For sub-7nm FinFET technologies, MOL shorts such as contact to gate shorts are not visible at any time during the manufacturing process [1]. Similarly, via opens which frequently result from the interaction of lithography, etch, and fill, are often due to via voids, which are also invisible at the surface of the wafer (Fig.1). For such buried defects, optical bright field defect inspection tools are not adequate. While the standard e-beam tools are capable of detecting these defects, their throughput is not sufficient (even for the multibeam tools) for the detection of parts per billion (PPB) defect levels [2].

Yield learning cycles involve detecting an issue, quantifying its impact, diagnosing the root cause, implementing a corrective measure, and validating the corrective measure. Yield learning cycles that rely upon full wafer processing and end of line testing are inherently slow – often measured in cycle times of several quarters. Furthermore, end of line testing confounds all systematic and random yield loss sources, thereby making it difficult to assess the impact of a specific (non-random) yield issue. The ability to detect and characterize yield loss issues inline (down to PPB level) is crucial to overcome this yield learning cycle bottleneck.

This work presents e-beam tool (eProbe 250) and the DFI system that have been built and deployed by PDF to address these critical needs. We then review defect inspection applications of this system: DirectScan and DFI Filler Cell inspection, and finally present the overlay process window characterization.

eProbe®250 e-beam System

The eProbe®250 e-beam system is designed, produced, and offered by PDF Solutions. The eProbe®250 system is tuned to perform voltage contrast (VC) measurements using vector scanning mode. By operating in vector scanning mode, the system is able to dedicate all the e-beam measurement time to measuring locations on the wafer that actually matter. The software embedded in the eProbe®250 system performs real-time registration during measurement and employs an artificial intelligence-based system for learning the relationship between the IC layout and the measured gray level signals, translated into an Electrical Response Index (ERI), used to identify defective sites on the wafer.

The throughput of the eProbe®250 is dictated by the field of view (FOV) and the stage speed. In most cases it operates with a FOV of 45 um x 45 um and can travel at a stage speed up to 100 mm / sec. The resulting throughput enables full wafer scans within 2-4 hours, therefore the tool is suitable for high volume production mode where queue time limitations impose stringent time constraints.

This throughput is enabled by the vector scan capability of the system and the associated software system. The eProbe®250 architecture provides a scalable trajectory for achieving throughput improvements in contrast to multi-beam e-beam systems which rely upon adding beams to achieve sub-linear throughput scaling at the expense of super-linear processing of test data.

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DirectScan

The goal of the DirectScan application is to inspect a given layer of a product to detect yield and reliability relevant defects [3]. The eProbe®250 has successfully measured layers with feature sizes as small as 1x metal layers in 4nm technology. DirectScan work flow consists of four stages as depicted in Figure 2. The first step is to identify a fail mode or set of fail modes of interest. This step dictates the layer at which the given wafer will be scanned. The second step consists of analyzing the product layout and generating the measurement recipe. PDF's proprietary FIRE software is used to analyze the product layout. This software identifies electrically relevant layout patterns for the selected fail modes. The next step is the actual measurement of the wafer on the eProbe®250. The final step is the analysis of the resultant data.

As an application example, DirectScan was used to identify high risk layout constructs in the products metal layers on a product manufactured in 7nm technology. Over 20 billion instances of layout patterns were scanned at the selected metal layer using VC measurement. Dark defects were measured and recorded such as the defect shown in Figure 3.

By running DirectScan, the impact of specific types of defects can be observed and quantified directly at the metal layer of interest which speeds up the diagnosis by several weeks.

Design-for-Inspection™ (DFI)

Most chips designed for advanced nodes consist of 5-15% empty space in the standard cell layers. This space represents an opportunity to instrument chip designs with e-beam testable test structures (which we refer to as "DFI Filler cells"). Within standard cell regions, these DFI Filler cells look similar to the conventional filler cells, except they are modified to be sensitive to a particular fail mode of interest and include an eProbe test pad for high throughput measurement (Fig. 4).

Insertion of DFI Filler cells is transparent to existing design flows. DFI Filler cells are swapped in place of the conventional filler cells. DFI Filler cells are selected to provide observability for critical fails modes. In addition to detecting shorts and opens, the DFI Filler cells excel at detecting leakages that represent soft shorts which often correspond to reliability weakness [4].

In addition to inserting DFI Filler cells within logic blocks, DFI structures can be inserted in the gaps between logic blocks. These inter-block space regions tend to provide contiguous chunks of area that can be used for special DFI structures that require larger footprint than what is compatible with dimensions of the standard cell.

In-Line Monitor of Overlay and Process Window

Another application area for DFI structures is within scribe lines. Although scribe lines represent a scarce amount of area, they offer an opportunity to insert DFI structures with pushed design rules. Such structures can be used to characterize the overlay and process window margins for all critical layers [5]. An example of such application is shown in Fig. 5.

Conclusions

The DirectScan and DFI applications are revolutionizing the best in class practices for inspecting sub-surface defects at PPB levels of statistical significance. These capabilities are enabled by the eProbe®250 hardware. The resulting system provides faster yield learning loops which are critical for the types of defects that are limiting yields at advanced nodes. The system has been deployed at multiple foundries across multiple products. Critical systematic yield loss sources have been discovered with the DirectScan. The DirectScan and the broader set of DFI applications presented in this paper have the opportunity to advance the state of the art of the in-line control, diagnostics, and Failure Analysis.

References

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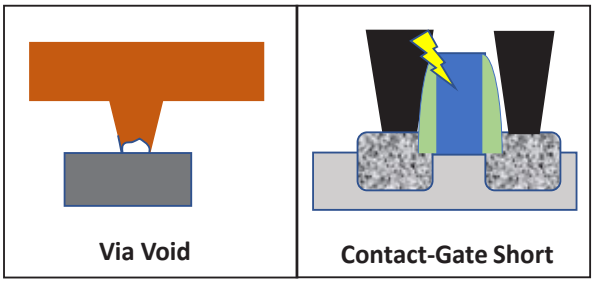

Fig. 1. Invisible Buried Defects

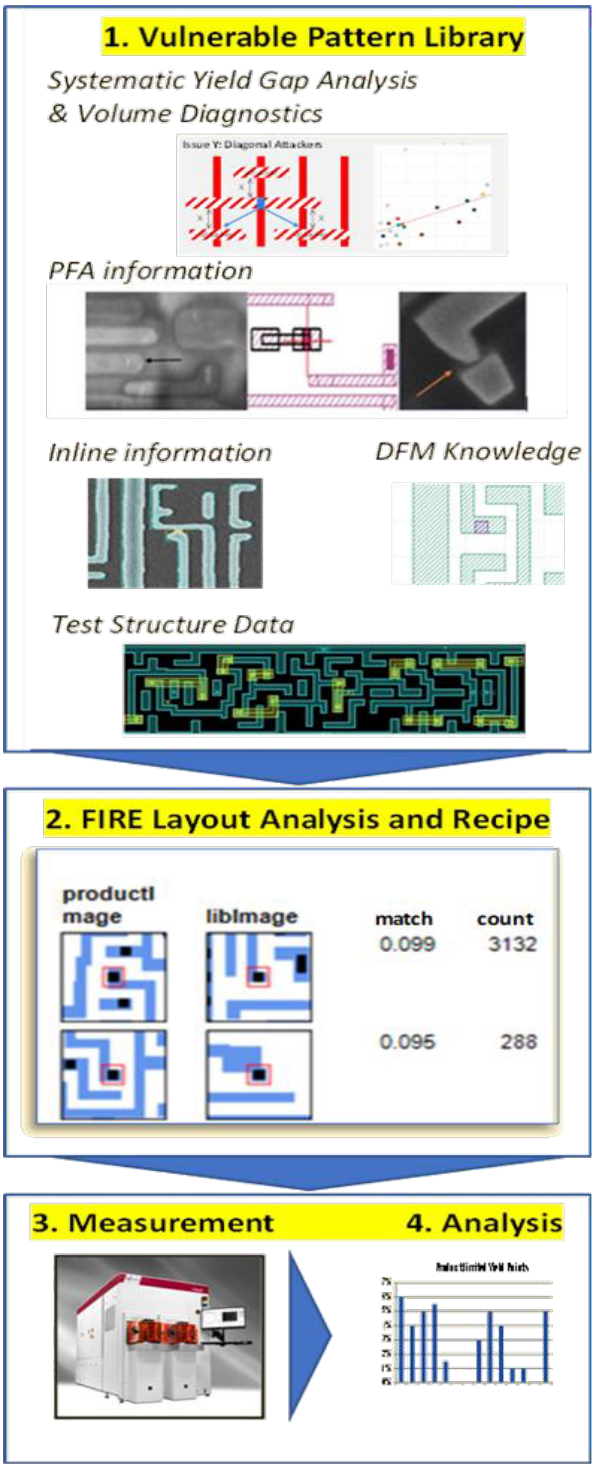

Fig. 2. DirectScan work flow

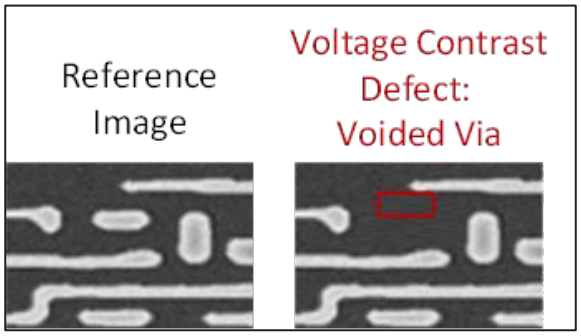

Fig. 3 Voltage contrast detected defect (buried Via void)

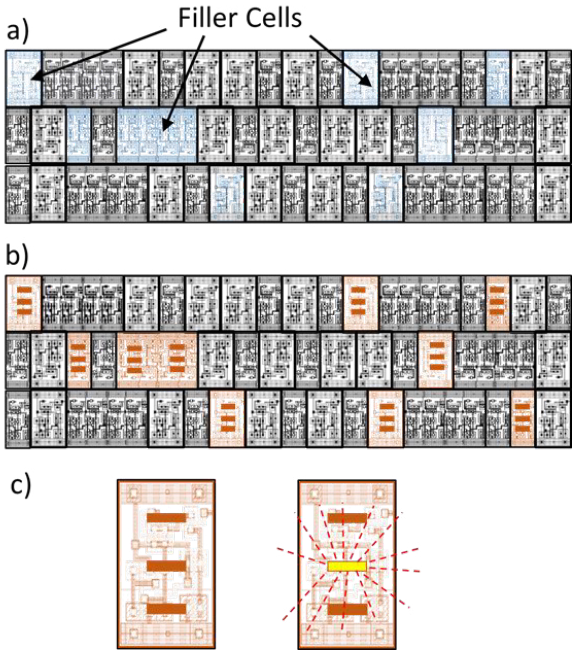

Fig. 4. a) Logic Block with Standard Cells and Filler Cells; b) The same block with redesigned Filler Cells, instrumented with DFI test structures and e-beam pads; c) Example of failure detection with e-beam test pad embedded in a Filler Cell

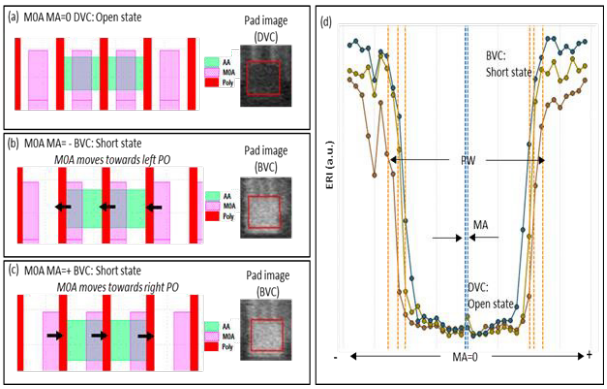

Fig. 5. Misalignment measurement using DFI and Process Window calculation using VC inspection